

### Scalar Operation

$$\begin{array}{ccccc} \boxed{A_x} & + & \boxed{B_x} & = & \boxed{C_x} \\ \boxed{A_y} & + & \boxed{B_y} & = & \boxed{C_y} \\ \boxed{A_z} & + & \boxed{B_z} & = & \boxed{C_z} \\ \boxed{A_w} & + & \boxed{B_w} & = & \boxed{C_w} \end{array}$$

### SIMD Operation of Vector Length 4

$$\begin{array}{c} \boxed{A_x} \\ \boxed{A_y} \\ \boxed{A_z} \\ \boxed{A_w} \end{array} + \begin{array}{c} \boxed{B_x} \\ \boxed{B_y} \\ \boxed{B_z} \\ \boxed{B_w} \end{array} = \begin{array}{c} \boxed{C_x} \\ \boxed{C_y} \\ \boxed{C_z} \\ \boxed{C_w} \end{array}$$

Intel® Architecture currently has SIMD operations of vector length 4, 8, 16